Position Sensitive Radiation Detector Integrated with an FPGA for Radiation Tolerant Computing

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***Abstract*— A position sensitive radiation sensor was modeled, developed and fabricated then interfaced with a field programmable gate array (FPGA) to create a radiation hardened computing platform. The system exploits environmental information from the sensor in order to determine regions within the FPGA that may have been affected by radiation. The spatial radiation sensor provides the computer system with the location of radiation strikes. This information is used by the computer system to avoid and repair effected circuits on the programmable fabric. By giving the recovery circuitry insight into the location where a fault may have occurred, the latency between detection of a fault and repair can be reduced. This provides an additional level of reliability by more efficiently detecting and correcting faults in SRAM-based FPGAs faults compared to the traditional voting and sequential search approaches.**

I. INTRODUCTION

The detrimental effects that cosmic radiation has on digital integrated circuits (ICs) can be classified into two categories; (1) Total Ionizing Doze and (2) Ionizing Radiation Transients [1,2]. Both of these effects come from the same physical phenomenon of radiation particles passing through the semiconductor material and creating an ionized electron/hole pair. Total Ionizing Doze (TID) effects result from charge carriers getting trapped in the insulating material of a transistor. When an electron/hole pair is created by the radiation strike (typically low energy electrons and protons) the carriers attempt to move back together to find an electrostatic equilibrium. Due to a difference in mobility rates in the semiconductor material, charge carriers can get trapped in the insulating material of the device. This can lead to threshold shifting and increased leakage current and results in permanent damage to the device.

Ionizing radiation transients are radiation strikes (typically from heavy ions and protons) that by themselves do not cause permanent damage to the materials in a device but do result in a charge accumulation in the diffusion region of the transistor. The ionization of the diffusion region causes free charge to be created. If this charge has a large enough magnitude, it will produce a voltage that can be observed as a state change by a receiving gate. This type of event, known as a single-event transient (SET) can lead to a logical failure called a Single-Event-Upset (SEU) when the state change is captured in a digital storage device. SETs and SEUs are referred to as a soft faults because no permanent damage is caused in the circuit [3,4].

Circuits can be *hardened* to withstand a certain level of TID. The likelihood of charge carriers getting trapped in the gate insulator of a transistor diminishes as the oxide thickness gets thinner. The susceptibility to oxide doping has been inherently lowered through the reduced feature sizes that modern fabrication processes are yielding. Techniques to reduce the impact of increased leakage current due to charge carriers getting trapped in the substrate include deep isolation trenches, intentionally doping the substrate, and enclosed transistor layouts. TID hardening has been around since the 1970s due to demand from the military and aerospace sectors. It should be emphasized that TID hardened parts are still susceptible to SETs from heavy ions and protons.

Digital circuits can be made *tolerant* to SETs and SEUs using logical mitigation approaches. One common approach is through the use of triple modular redundancy (TMR). In this approach, three identical circuits are used for each logic operation and the outputs are fed into a majority voter circuit. The voter produces the most common results which can overcome an SET in one of the circuits. TMR can also detect SEUs and produce the correct results. For SEUs, the memory device ultimately needs to be reset or reinitialized to remove the fault.

The use of FPGAs as the hardware fabric for military and aerospace computers has received great attention recently due to the improved computational performance that can be achieved and the inherent flexibility of the device. Hardware accelerated computing architectures implemented on FPGAs have been demonstrated by a number of research groups that

are capable of several orders of magnitude speedup and substantial energy saving over microprocessor implementations for equivalent algorithm execution [5-9]. When this is coupled with the ability to dynamically reconfigure, the practical deployment of high performance, reconfigurable computers becomes a reality. A reconfigurable computer (RC) is a system which reprograms its hardware during normal operation in order to accomplish the task at hand. RC can be used to achieve increased computation, reduced power, functional consolidation, or dynamic fault mitigation deployment. FPGA-based reconfigurable computers are becoming even more practical with recent efforts in making the circuit fabrics TID hardened [10]

RC computers implemented on FPGAs require that the hardware configuration be stored in a reconfigurable memory device. The most common and fastest reconfigurable memory used in FPGAs is SRAM. While SRAM-based FPGA are extremely attractive from an RC perspective, they are susceptible to additional fault conditions. If an SEU occurs in the configuration SRAM of the FPGA, a simple reset will not remove the fault because the physical hardware of the circuit has been altered. This is referred to as a Single Event Functional Interrupt (SEFI) because the damage cannot be recovered through normal circuit operation. To recover from a SEFI, the configuration SRAM must be reinitialized. Typical SEFI detection and mitigation is accomplished using a circuit called a *scrubber*. A scrubber is a circuit which sequentially compares the contents of the configuration SRAM to an off-chip, non-volatile memory device holding the original contents.

One disadvantage of traditional scrubbers is that they search the configuration memory in a sequential manner. This can lead to significant latencies between the fault occurrence and fault detection. Furthermore, the re-initialization of the FPGA typically is done on the full chip which leads to a significant performance hit during repair.

In this paper, we present a logical fault mitigation approach for SEUs and SEFIs using a spatial radiation sensor. Since the configuration SRAM is distributed within the circuit fabric, if the spatial location of a radiation strike can be determined, then the location within the configuration SRAM that may have been affected can be determined. We present the design of a spatial radiation sensor that can detect the XY location of radiation strikes at levels that cause SETs/SEUs/SEFIs in modern FPGA processes. This sensor is designed to be packaged on-top of the FPGA to provide spatial information about which areas of the substrate may have been hit. A redundant, many-core computer architecture has been developed to exploit the spatial information from the sensor in order to avoid and repair effected regions of the FPGA. This approach has the potential to deliver a logical approach to fault mitigation in SRAM-based FPGAs with increases performance and reduced recovery latency.

II. REDUNDANT MANY-CORE ARCHITECTURE

In our approach, an FPGA fabric is divided into equally sized homogenous tiles. Each tile is sized such that it can contain an entire soft processor and be partially reconfigured. Partial reconfiguration (PR) involves reinitializing only a section of the configuration SRAM on the FPGA. At any given time, three of the soft processors are configured in TMR with the rest of the processors available as spares. In the event that the TMR voter detects a fault, the two good processors complete their current task and then prepare for a reset/resynchronization procedure by off-loading their variable data to a recovery system. The recovery system then brings a spare processor online to replace the effected tile. The three active processors are brought out of reset and immediately read in the variable data into their RAM and continue operating their main routine. Processors that are not used are held in reset to save power. Processors are brought online by de-asserting their reset line. A system log is maintained that tracks which processors have been faulted. Once the three active processors are online and running in the foreground, the recovery system initiates partial configuration on the effected tile to repair the damaged circuit. The PR of the tile repairs SEFIs while resetting the tile will repair SEUs.

Care must be taken when conducting PR to not cause faults to the rest of the system while the hardware is being reprogrammed. We avoid this obstacle by only conducting PR on non-active processors.

This procedure can also be triggered by the external radiation sensor. If the sensor detects a fault, it sends the spatial location of the strike to the recovery system. The recovery system has a map that matches the XY location of the strike to the tile within the many-core system and also to the addresses within the configuration SRAM that correspond to that tile. If the effected processor is active, the system undergoes a recovery procedure outlined above. If the effected processor is a spare, it is partially reconfigured without impacting the processors running in the foreground. Using environmental information from a sensor has an advantage over TMR by itself. First, faults in non-active circuitry can be detected and repaired prior to being used. Second, active circuitry that is currently not in use, such as future states in a state machine, can be repaired before the microprocessors undergoes a severe system level fault.

We have prototyped our computer architecture on a Xilinx Virtex-5 LX110 FPGA using the Xilinx *picoBlaze* soft processor [11]. When considering the resources for the picoBlaze processor and constraints of the PR tool, it was found that 16 soft processors could be implemented on this FPGA. Each of the 16 processors contain the same software to control a set of basic peripherals (PS2 mouse, PS2 keyboard, and LCD). We monitored the logical operation of the system using the Xilinx ChipScope Logic Analyzer. This tool allows the digital signals of any internal node to be observed. Fig. 1 shows the floor plan of the FPGA with the location of the 16 processors outlined. Also shown is a zoomed in view of a tile highlighting the resourced that are refigured during PR. The picoBlaze processors takes 24 CLBs and 1 BRAM. The constraints of the Xilinx PR tool dictate that the PR tile must be larger than the picoBlaze circuit.

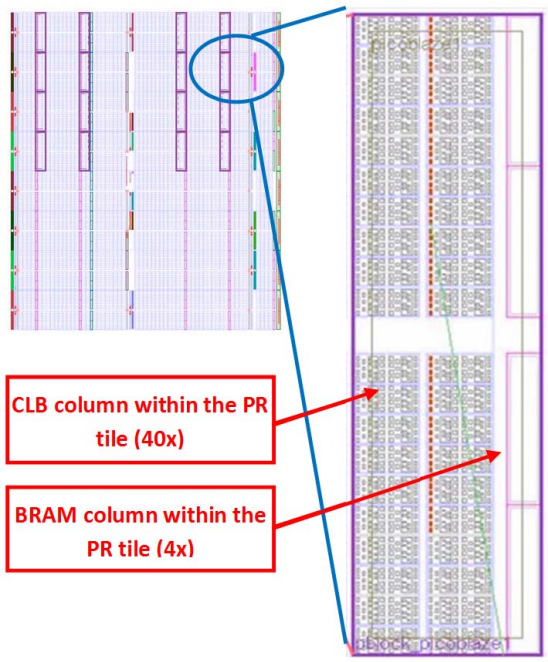

Fig. 1. Floor plan for the V5-LX110 FPGA highlighting the 16 reconfigurable tiles each containing a PicoBlaze processor in addition to a zoomed in view of the PR tile used in this work highlighting the constraints of partial reconfiguration.

III. Spatial Radiation Sensor Design & Fabrication

A. Design

We have designed and fabricated a sensor based on techniques and practices developed for use in nuclear spectroscopy experiments. In the field of elementary particle physics it is necessary to take very fast and precise position measurements to monitor very rare and short lived ionizing particles produced in particle colliders [12-14]. Semiconductor radiation sensors have been developed to monitor the paths of these particles as they exit a reaction. Conversely, we are developing the same techniques to monitor position and energy of ionization radiation as it enters electronics for space systems.

The wafers were processed at the Montana Microfabrication Facility on the campus of Montana State University. Lightly doped n-type double-side polished silicon wafers were wet oxidized at 1000°C for 90 minutes. The wafers were coated with photoresist on both sides and the p+ areas were opened by standard photolithography methods. The photoresist was removed and the wafers were doped using solid source pre-deposition methods. The masking silicon dioxide was stripped and new oxide was grown using the same oxidation parameters. Windows were opened for the n+ areas and a solid source pre-deposition was preformed. The masking dioxide was again stripped and new dry oxide was grown at 1000°C for 60 minutes. Windows were then opened in the oxide over the contact areas. Aluminum was evaporated onto one side of the wafers and patterned to make the collecting electrodes. The opposite side was then metalized with aluminum then both sides of the wafer were covered with photoresist. Collecting electrodes were then patterned orthogonal to the previous pattern on the opposite side of the previous pattern. The photoresist was removed from both sides and the wafers were cleaned and annealed at 450°C for 20 minutes.

The prototype sensor was designed to operate with a 1064nm infrared laser. At this wavelength silicon has an absorption coefficient that allows the IR radiation to penetrate to the opposite side of the 525 micron thick sensor. Charge can then be collected on each side of the orthogonal grid pattern that positions the radiation strike to the intersection of the peak current collected on electrodes on opposite sides of the sensor.

Fig. 2 shows the cross-section of the fundamental sensing element, a pn junction used as a radiation detector. The ionization radiation passes through the sensor creating electron hole pairs on an average energy rate of 3.6 eV per electron-hole pair. In silicon, 1 MeV of energy corresponds to 44.4 fC of charge, which is more than enough to flip the state of a logic circuit fabricated in a modern process [12-14]. Within a diffusion length of the depletion region, the intrinsic electric field sweeps the charges toward their corresponding electrodes, electrons to the n+ side of the substrate and holes to the opposite p+ side. The energy of the radiation and the size of the depletion volume determine the amount of charge ultimately collected which is a function of the sensor design, materials, and bias voltage.

There have been numerous sensor designs for monitoring position and energy of radiation with variations in resolution and system integration [15-17]. We have selected to develop double sided strip detectors and silicon drift detectors for this project for their simple design, speed and ease of production but without sacrificing position and energy resolution [18]. The principle of the strip detector is very simple. It is based on a large area pn diode, very similar to a solar cell. The difference stems from the electrodes in the radiation sensor, which are broken up into narrow strips running orthogonal to each other on both sides of the substrate, each of them being read-out with a separate electronic channel. The location of the ionizing radiation is given by the position of the intersection of the strips receiving the signals from the front and back electrodes (Fig. 2). Fig. 3 shows the actual sensor.

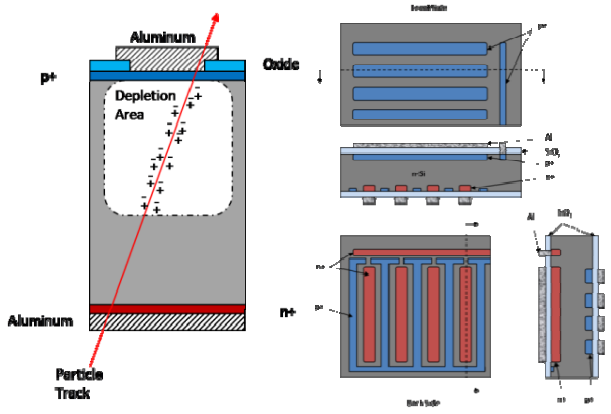

Fig. 2. Cross-section of detector and layout of strip detector.

Fig. 3. Prototype of fabricated sensor on package carrier

B. Modeling

We developed numerous finite element models of radiation sensors with radiation strikes to aid in the development and design of the radiation sensor. All are based on Maxwell's electrostatic equations and Boltzmann transport theory. Three application modes in COMSOL Multiphysics were used to define the model. Electrostatics governs the electrical interaction between charges and separate domains for the convection and diffusion of holes and electrons were used. Various geometries of doped areas were approximated by Gaussian functions that created internal electric fields and depletion regions, which could be modified by applying biasing potentials on boundaries of the models. The results of the biased diode models were then perturbed by adding a radiation strike to disrupt the equilibrium results. The radiation strike was modeled as a Gaussian distribution of generated electron hole pairs (EHP) on a trajectory that could be defined by initial parameters. The charge distribution was simulated as an average of 80 EHP generated per micron of silicon [19]. Fig. 4 shows a two dimensional cross-section of a fully depleted silicon sensor at various times after a radiation strike. The radiation strike creates the electron hole pairs that begin to separate due to the electric field within the silicon. The electrons and holes spread due to diffusion, with the electrons spreading more due to the higher mobility of the electrons. The top and bottom boundaries were integrated with respect to the charge flux to get a representation of the anticipated current pulse due to the electrons and holes (Fig. 5).

C. Characterization

The first tests of the radiation strip detector have been done by pulsing a 5mW Helium-Neon laser source onto the surface of the sensor. This gave confirmation of the functional operation of the detector integrated with the readout circuitry, by using photogeneration of electron-hole pairs rather than ionizing radiation to generate the charge signal. The laboratory setup shown in Fig. 6 was used to test the sensor. For this setup, the laser was positioned over a *target channel* (1-12) and the current and voltage were recorded on all the channels (*observation channels, 1-12).* This allowed us to see how large of a signal was created upon a direct strike and how much energy was inadvertently created on adjacent channels. Table I and II show the measured current and voltage for this setup. For the prototype sensor used in this characterization, channel 3 was non-functional.

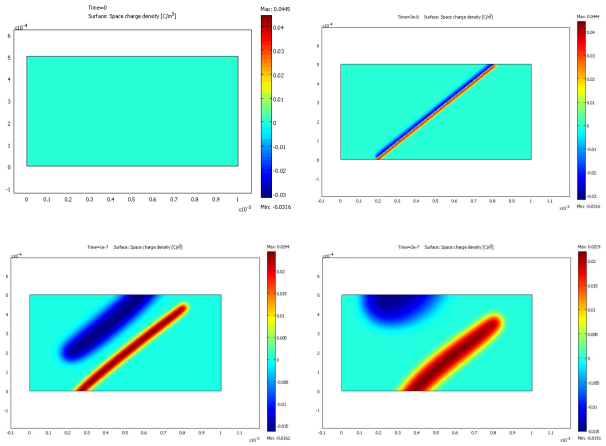

Fig. 4. COMSOL simulation of electron (negative-blue) and hole (positive-red) due to a single radiation particle strike. Upper-left shows the material prior to a strike. The Upper-right, Lower-left, and Lower-right shows the space charge densities at 30ns, 100ns, and 200ns respectively.

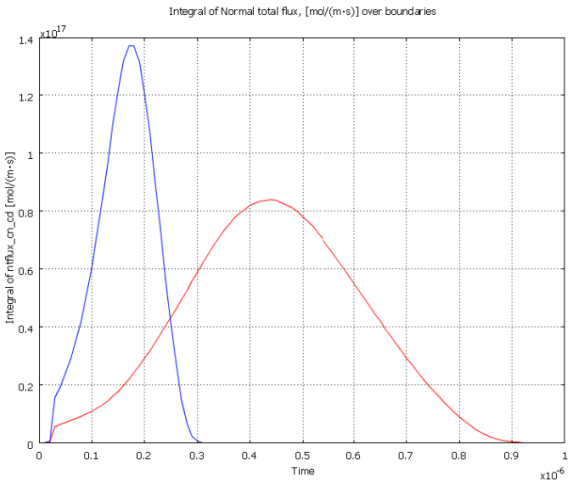

Fig. 5. Simulation of electron (blue) and hole (red) output pulse due to a single radiation particle strike.

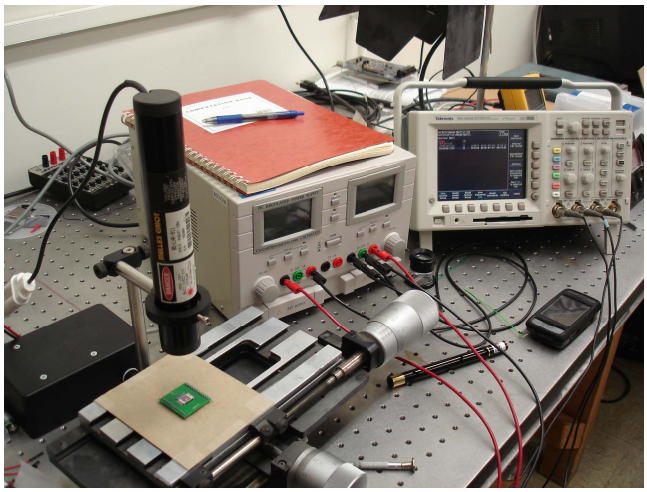

Fig. 6. Laboratory setup for sensor testing.

TABLE 1. CURRENT FROM 5mW HeNe LASER

I (uA)		Target Channel											
		1	2	3	4	5	6	7	8	9	10	11	12
Observation Channel	1	41	39	-	35	31	30	30	28	25	24	22	19
	2	37	43	-	38	33	32	32	29	27	25	23	19
	3	-	-	-	-	-	-	-	-	-	-	-	-
	4	32	35	-	40	36	34	34	31	28	26	24	20
	5	29	31	-	36	39	35	35	32	29	27	25	20
	6	26	28	-	33	35	36	37	34	30	28	26	21
	7	23	25	-	29	31	33	38	37	32	29	27	22
	8	19	22	-	26	27	29	35	41	34	32	28	23
	9	16	18	-	22	23	25	30	34	34	35	29	24
	10	14	15	-	19	20	21	26	29	30	40	32	27
	11	12	13	-	11	17	18	22	24	26	32	34	29
	12	11	12	-	9	15	16	19	21	23	27	30	31

TABLE 2. VOLTAGE FROM 5mW HeNe LASER

V (mV)		Target Channel											
		1	2	3	4	5	6	7	8	9	10	11	12
Observation Channel	1	146	142		127	113	109	110	104	94	90	84	70
	2	135	152		135	120	115	115	108	98	93	86	72
	3	-	-		-	-	-	-	-	-	-	-	-
	4	114	124		142	130	123	121	114	103	97	90	75
	5	103	113		132	139	127	127	118	107	100	92	76
	6	93	101		119	127	130	135	124	111	103	95	78
	7	82	90		106	112	118	138	134	116	108	98	80
	8	72	78		94	99	105	126	148	123	116	103	84
	9	62	68		82	86	92	109	123	121	129	108	89
	10	52	57		71	74	79	94	105	110	144	116	97
	11	44	48		60	63	68	81	89	95	116	122	106
	12	40	44		54	57	61	72	78	84	100	110	115

The second test of the sensor was performed by pulsing a 1064nm IR laser. Since IR is invisible to the human eye, a single channel was arbitrarily targeted and measurements were taken on the 12 topside observations channels. Fig. 7 shows the current and voltage levels for the observation channels indicating that the strike occurred on channel 8.

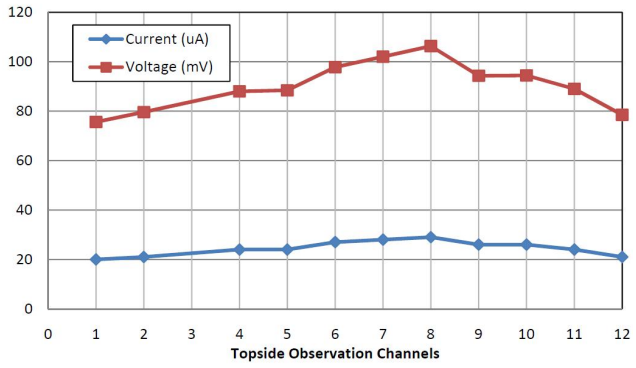

Fig. 7. Laboratory setup for sensor testing.

IV. SENSOR AND FPGA INTERFACE ELECTRONICS

A. Design

Electronics are needed in order to convert the small amount of current produced by the sensor (uA) to a signal suitable for detecting by the FPGA as a 1 or a 0. The first stage of the electronics consists of an integrator which produces a voltage level based upon the small current pulse produced by the sensor. A National Instruments LMV324 OpAmp was chosen due to its high slew rate and low input bias current. A variable reference voltage is used in this stage in order to compensate for ambient radiation during demonstration purposes.

The second stage consists of a non-inverting OpAmp. This stage contains gain that amplifies the integrator signal to a voltage that takes advantage of the entire dynamic range of the device. For the levels in our prototype, the gain is selected such that the outputs of a direct strike on a channel corresponds to a signal of 2.5v. Table III shows the gain used to normalize each of the topside channels Each channel of the sensor has a different gain setting in order to compensate for fabrication differences between the strip detectors. Again, an NI LMV324 is used due to its high slew rate.

The third stage consists of a comparator circuit designed with an OpAmp in an open-loop configuration. An NI LMH6601 part was chosen due to its small form factor. A variable switching threshold voltage is used in this stage to set the point at which the comparator will switch. This threshold is set at a level between the voltage on a channel due to a direct radiation strike and the voltage due to a strike on an adjacent channel. This allows the circuit to distinguish between a direct strike and parasitic energy on a neighbor.

TABLE 3. GAIN USED FOR NORMALIZATION

		Gain
		(v/v)
Channel	1	17.182
	2	16.437
	3	-
	4	17.668
	5	18.025
	6	19.216
	7	18.090
	8	16.915
	9	20.593
	10	17.361
	11	20.475
	12	21.815

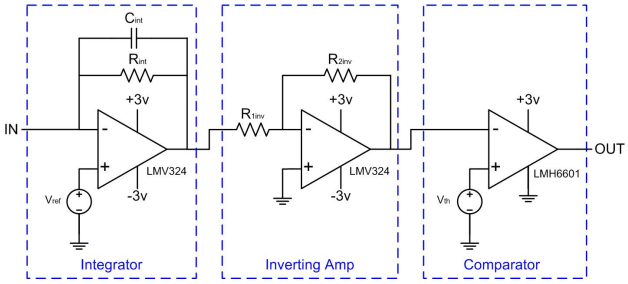

Fig. 8. Schematic for interfacing electronics.

B. Characterization

We used the 5mV HeNe laser to pulse the sensor in order to test the interface electronics. The laser was positioned on each channel in turn and all of the channels were observed with an oscilloscope at the output of the inverting OpAmp. The inverting OpAmps were normalized with the values in Table III. Fig. 9 shows the oscilloscope plots of the output of the inverting OpAmp in Fig. 8. On this plot is also shown the position of the v_{th} that would be used by the comparator stage to discern whether a strike occurred. The output of the comparator is fed into the FPGA in order to provide the computer system with a digital signal representing the XY coordinate of the strike.

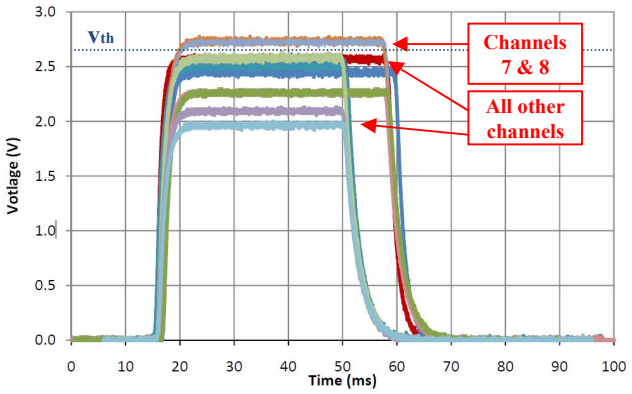

Fig. 9. Sensor pulse response of the system observed at the output of the non-inverting opamp.

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